	Experiment title: In situ X-ray diffraction study of epitaxial praseodymium oxide layers on Si(001) as alternative high-k dielectrics in future sub-µ CMOS technology	**Experiment number**: **SI-976**
Beamline: ID32	**Date of experiment**: from: Feb 18 to: Feb 24, 2004	**Date of report**: 21-02-2005
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Report:

The goal was to study the heteroepitaxial system Pr_2O_3/Si to gain detailed knowledge on the oxide/Si interface region as well as the oxide surface itself. Such studies are still needed before this oxide can be processed and the next step on the *I*nternational *T*echnology *R*oadmap for *S*emiconductors (ITRS) can be reached in time. Previous work demonstrated that (i) crystalline Pr_2O_3 layers of high quality can be grown on both Si(001)[1] and Si(111) [2] substrates ; (ii) this new heteroepitaxial system can be integrated in the process technology of new generations of microelectronics devices [3]. These experiments were performed ex-situ and thus the Pr_2O_3 films were covered by an amorphous Si capping layer of several nm thickness to protect the oxide layers from moisture.

This report presents the first results on the in-situ surface X-ray diffraction study of the structural properties of Pr_2O_3 thin films on Si(001) substrates, gaining insights in the initial stage of the formation of the oxide layer on the Si(001) substrate surface. During the beamtime allocated, we combined low energy electron diffraction (LEED), scanning tunneling microscopy (STM) and surface x-ray diffraction (SXRD) information to obtain a complete data set on this Pr_2O_3/Si(001) system. Experiments were performed in UHV from the growth to the final characterization. A critical part in these experiments was to get atomically clean Si(001) surface using a 2mm thick hat shape silicon crystal.

The solution for cleaning the silicon substrates is direct heating of the crystal by applying a metallic contact on both wings on the hat shape crystals (see Fig.1 below). The BTU Cottbus team developed the preparation chamber in which the depositions were performed.

Sample preparation was carried out in the surface characterization laboratory (SCL) of ID32. 10 samples, as the ones shown on Fig.1, have been prepared during the beamtime which had been cleaned by repetitive flash annealing treatments up to 1250°C. Oxide films were deposited with an e-beam evaporator. Pr_6O_{11} powder in a Mo crucible was reduced to get Pr_2O_3 evaporant. During deposition the sample was kept at T_{sample} at 550°C. The LEED patterns were always checked before and after deposition. Five of these samples were subsequently measured by XRD at ID32.

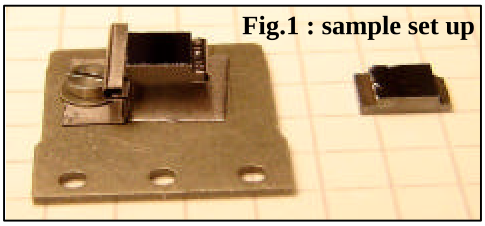

Fig.1 : sample set up

Fig.2 shows typical LEED patterns. Picture *a* shows a clean Si(001) surface with (2×1) reconstruction. Picture *b* is the LEED pattern obtained after deposition of about 1Å thick film: one can notice a higher background intensity and weaker spot intensity from the (2×1) reconstructions. Picture *c* is the LEED pattern obtained after having evaporated about 2Å more of Pr_2O_3 : only the (1×1) spots are visible.

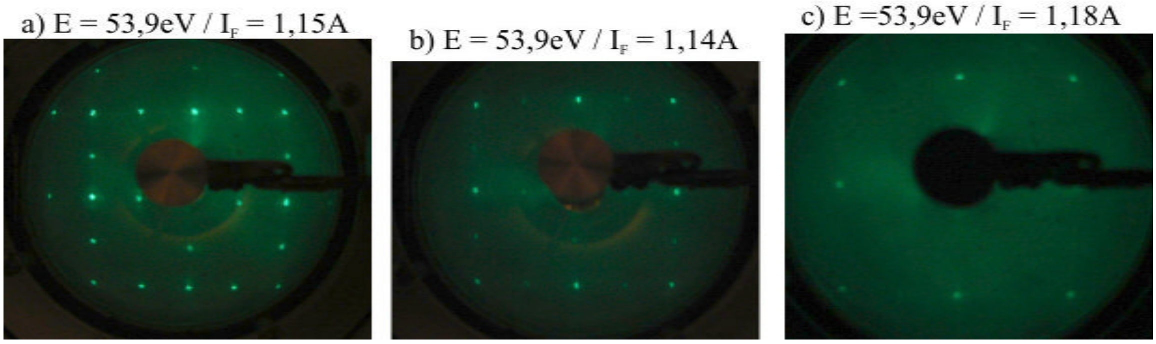

Fig.2 : LEED patterns performed on sample S1 :

(a)Clean Si(001) substrate; (b)1Å thick Pr_2O_3 film on Si(001); (c)2Å more of Pr_2O_3 on same sample

The samples were transferred into the ID32 UHV baby chamber and X-ray diffraction measurements were carried out with the ID32 multi-circle Huber diffractometer.

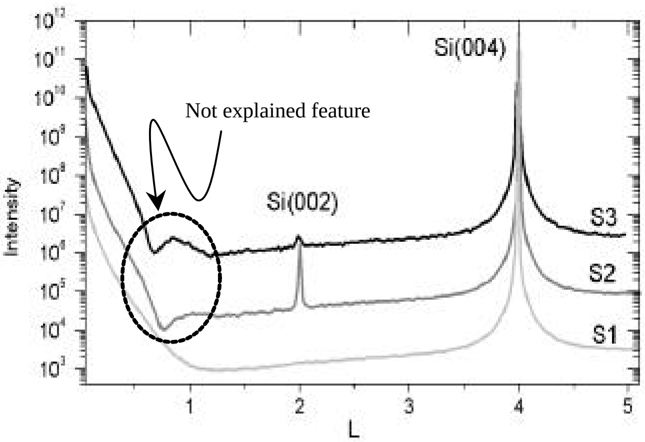

Fig.3 : Reflectivity scans

Fig.3 shows reflectivity scans, along the specular CTR (00L) rod. These scans do not show clear evidence of the presence of Pr_2O_3 film. We however see some modulations at low L values (L<1). Also indication of a rough interface is visible at higher L values.

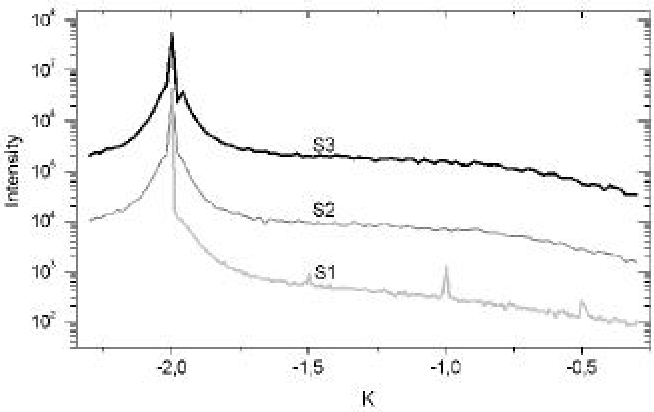

Fig.4 : In-plane scans along K direction.

In-plane scans shown in Fig. 4 did not give evidence of a crystalline film. No in-plane diffraction peaks from the file are visible.

CTR measurements along the <20L> rods, as shown on Fig. 5, indicate a rough substrate / film interface. But no peaks coming from the Pr_2O_3 film (only peaks coming from the silicon substrate). Simulations are being carried out to quantify the roughness on these surfaces.

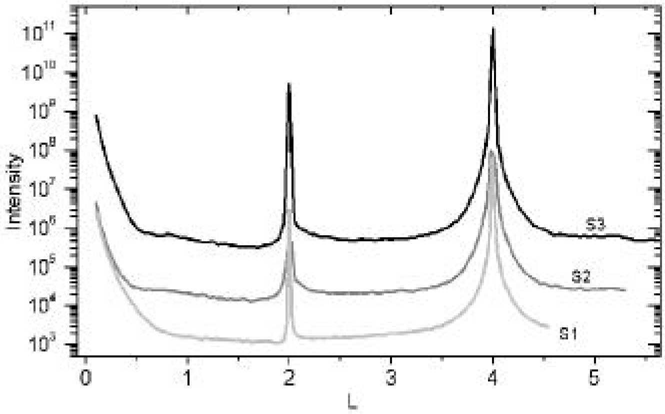

Fig.5 : <20L> scans.

After the regular beamtime ended, the samples were transferred back into the UHV system in the SCL and characterised with STM.

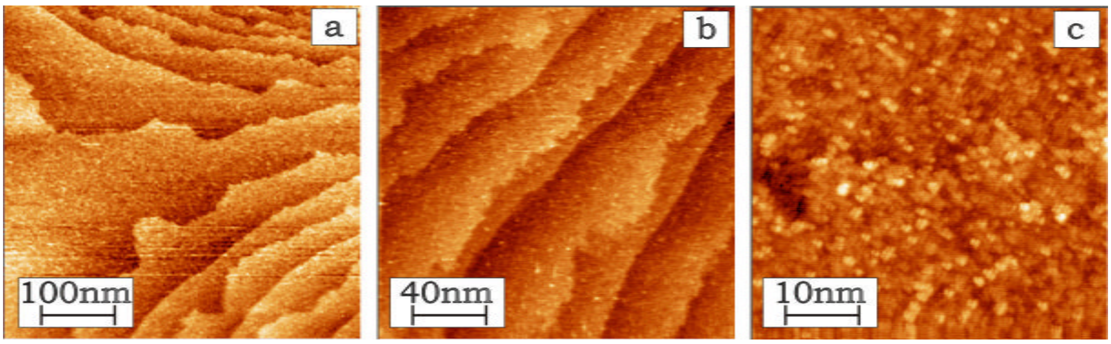

Fig.6 : STM measurements of a direct heating cleaned Si(001) hat shape crystal.

(a) 500×500nm^2, U_s = 1.5V ; I_t = 0.2nA

(b) 200×200nm^2, U_s = 1.5V ; I_t = 0.5nA

(c) 50×50nm^2, U_s = 2V ; I_t = 1 nA

The LEED, STM and SXRD data are presently still analysed to obtain information about the structure of the ultrathin oxide film and its interface with the Si(001) substrate.

[1] T. Schroeder, T.-L. Lee, J. Zegenhagen, C. Wenger, P. Zaumseil and H.-J. Müssig, APL **85** (2004) 1229

[2] T. Schroeder, T.-L. Lee, L. Libralesso, J. Zegenhagen, P. Zaumseil, C. Wenger, H.-J. Müssig, J. Appl. Phys., accepted

[3] U. Schwalke, K. Boye, K. Haberle, R. Heller, G. Hess, G. Müller, T. Ruland, G. Tzschöckel, H.J. Osten, A. Fissel, and H.-J. Müssig, *Proceedings of the 32nd ESSDER*C, Firenze 2002, p407