

## Experimental report: 02 02 721 - SI 1691 (BM02)

### Strain in reverse embedded SiGe structures

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Samples from CEA-Leti.

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Round 07/2008

Elastic strain is nowadays commonly used in silicon layers to enhance carrier mobility of silicon microelectronics devices. In the literature, two main ways have been explored to stress the silicon active layers. The first solution consists in using process-based induced stress, for example contact etch-stop layers or SiGe Source/Drain [Eneman05], whereas the second one uses a global stress imposed by the substrates [Currie01]. With the continuous reduction of the channel dimensions, we have to check that the strain is maintained in the channel after the critical integration processes, especially after patterning. During our previous experiments, we studied strained-Silicon obtained by the growth on SiGe alloys and wafer bonding transfer to get simple sSiOI structures. The present experiments have been mainly focused on the measurement of the “reverse embedded SiGe structures” initially proposed by IBM [Donaton06] and shown in Fig. 1. The advantage of reverse embedded SiGe structures relies on the fact that the strain is increased for smaller channel dimension, i.e. when it is necessary to compensate mobility degradation, contrary to the global stress techniques which is less efficient for small patterns.

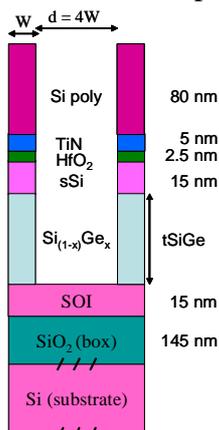


Fig.1: Schematics of studied samples. The top sSi corresponds to the channel material under investigation.

SiGe width (nm)	100	x	x	x		x	x
200					x		
Ge fraction (%)	20	x	x	x	x		
30						x	
45							x
SiGe thickness (nm)	20	x					
30				x	x	x	x
40			x				

Table1: Parameters of the measured samples. These samples correspond to model structures used in transistors.

The samples are obtained by the following way in CEA-Leti. A  $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$  bilayer was first grown in eptaxy on a SOI substrate, followed by gate stack deposition ( $\text{HfO}_2$  gate oxide and TiN/Si poly gate), the next step being the gate patterning. The  $\text{Si}_{(1-x)}\text{Ge}_x/\text{Si}$  bilayer is then

etched, allowing the SiGe compressive layer to relax. This relaxation creates a **tensile** strain in the Si channel layer.

To measure the strain by GIXRD in such samples, we have patterned 4 mm long lines of small width ( $W=100$  and  $200$  nm) by e-BEAM photolithography and etching (cf. Fig.1). The stress transfer depends on geometrical dimensions [Fiorenza08]. In this work, we have investigated the influence of three key parameters (using the samples described in Table1): the Ge fraction of the SiGe layer that determines the maximum value of strain that could be transferred to the Si layer, and two geometrical dimensions to study the efficiency of the stress transfer: the SiGe layer thickness  $t_{\text{SiGe}}$ , and the width  $W_{\text{SiGe}}$  of the lines that corresponds to the width of the SiGe embedded region.

The X-ray energy is 11 keV. Grazing incidence ( $\alpha_i=0.2^\circ$ ) and emergence angles ( $\alpha_f=0.4^\circ$ ) close to the critical angles of total reflection allow measuring the diffraction of planes perpendicular to the surface for the sSi/SiGe/SOI stack as well as for the Si substrate. Larger grazing angles ( $\alpha_i=0.3^\circ$ ,  $\alpha_f=0.6^\circ$ ) are used to go through the amorphous oxide layer (BOX) (145 nm thick). The Si substrate gives an internal stress-free reference in the samples both in position and width allowing to check the setup alignment, the resolution function, and to decrease the error bar of the strain measurement. The gate stack HfO<sub>2</sub>/TiN/Si poly has an impact on the strain state but does not absorb too much the beam.

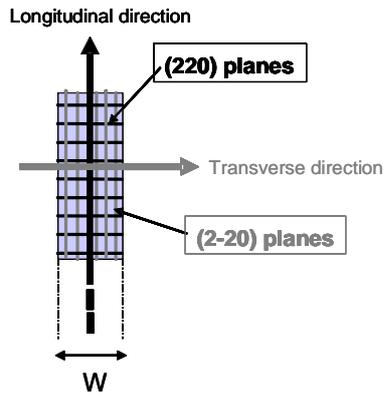


Fig.2 : Strain measurements directions and corresponding crystallographic planes.

The radial ( $\omega$ - $\psi$ ) scans enable the measurements of the lattice planes  $d_{Si,sSi}$  for Si and sSi (strained silicon layer) at a given  $\{hkl\}$  reflection and therefore the estimation of the strain  $\epsilon^{\{hkl\}} = (d_{sSi}^{\{hkl\}} - d_{Si}^{\{hkl\}}) / d_{Si}^{\{hkl\}}$ . The  $\psi=2\theta_B$  Bragg peak angles of the sSi layer and substrate are obtained by the optimization of intensity with radial and transverse scans at given grazing angles. Applying the Bragg law  $2d_{\{hkl\}} \sin(\theta_B) = \lambda$  (with  $\lambda$  the X-Ray wavelength) to the sSi and Si substrate layers, we get

$$\epsilon^{\{hkl\}} = \frac{\sin(\psi_{Si}^{\{hkl\}} / 2)}{\sin(\psi_{sSi}^{\{hkl\}} / 2)} - 1 \quad (1)$$

This equation shows that the strain can be directly deduced from the detector angular position  $\psi_{sSi}^{\{hkl\}}$ , whereas  $\psi_{Si}^{\{hkl\}}$  can be measured under identical experimental conditions or directly deduced from the Bragg law.

By convention (see Fig.2), the measurement of the (220) planes allow getting the strain in the long line direction, whereas the (2-20) planes give the strain in the direction perpendicular to the line.

We study first the influence of the SiGe layer thickness for a fixed Ge fraction (20%) and SiGe width ( $W_{SiGe}=100$  nm). The radial ( $\omega$ - $\psi$ ) scans corresponding to the (2-20) crystallographic planes have been plotted on Fig. 3 for three different SiGe layer thicknesses (20, 30, 40 nm). The broad Bragg peaks correspond to the Si/SiGe/Si stack, and the Si substrate reference is also been plotted on the same graph. These graphs allow getting the transverse strain perpendicular to the lines for the different SiGe thicknesses. The radial scans corresponding to the (220) crystallographic planes have been plotted in the inset of Fig. 3 for the three SiGe layer thicknesses and the Si substrate. They allow getting the longitudinal strain along the lines. For the (220) planes (corresponding to the long line direction), the Bragg peaks corresponding to the different SiGe thicknesses are close to the Si substrate angular position. That means that the strain along the line is very small whatever the SiGe thickness. For the (2-20) planes (corresponding to the line width direction), the Bragg peaks of the different SiGe thicknesses are shifted from the Si substrate Bragg peak position. They have a smaller  $\psi$  angle, meaning that the strain induced in the lines in the transverse direction is **tensile**. The shift from the Si substrate is larger for increasing SiGe thickness, which means that the strain is greater when the SiGe thickness increases. Simulations will be necessary to separate the contributions of the Si/SiGe/Si layers. *Qualitatively, we can nevertheless conclude that the stress transfer is more efficient with a thicker SiGe layer for the same Ge fraction and SiGe width.*

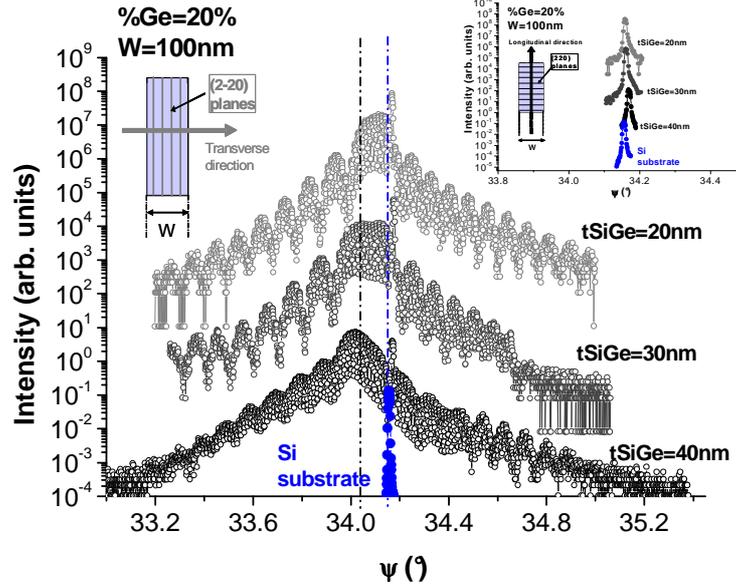


Fig.3: (2-20) Bragg peaks of the Si/SiGe/Si stack (20%Ge, WSiGe=100 nm, tSiGe=20, 30, 40nm) and unstrained Si substrate. Inset: (220) Bragg peaks.

Then, we studied the influence of the Ge fraction for a fixed SiGe thickness ( $t_{\text{SiGe}}=30\text{nm}$ ) and a fixed SiGe width ( $W_{\text{SiGe}}=100\text{nm}$ ). We have plotted in Fig. 4 the Bragg peaks corresponding to the (2-20) planes for three different Ge fractions (20%, 30% and 45%) and in the inset of Fig. 4 the (220) peaks. As previously observed, the strain is very limited along the long line direction, and for the smaller direction, the peak position shifts from the Si substrate toward smaller Bragg angles indicate that the Si is more tensile with larger Ge content. We can also see on these graphs two different contributions probably corresponding to the SiGe/sSi bilayer and to the bottom SOI layer. The contribution that shifts from the Si substrate toward smaller Bragg angles corresponds to the SiGe/sSi stack. The etching of the SiGe/sSi stack relaxes the SiGe compressive layer that recovers its lattice parameter. It explains the increase of the shift from the Si substrate with the Ge fraction. The etching-induced SiGe compressive layer relaxation transfers tensile strain to the Si free top layer in the small line direction. Another relaxation mechanism takes place during etching. Since the width of the line is very small (100 nm), the tensile strain introduced in the Si layer tends also to relax because of the free edges of the line (as observed in the more simple bonded sSi lines). The asymmetry of the curves should be explained by this non uniform strain in the width line direction. The contribution of the Bragg peak remaining at the Si substrate position corresponds to the SOI bottom layer. This layer is not influenced by the stress transfer mechanism because of the presence of the BOX and the absence of free edges. We have here qualitatively described Fig. 4 but detailed mechanical simulations and diffraction profiles simulations will be performed to give better understanding of these results and extract strain values in the sSi layer which are relevant for transport properties.

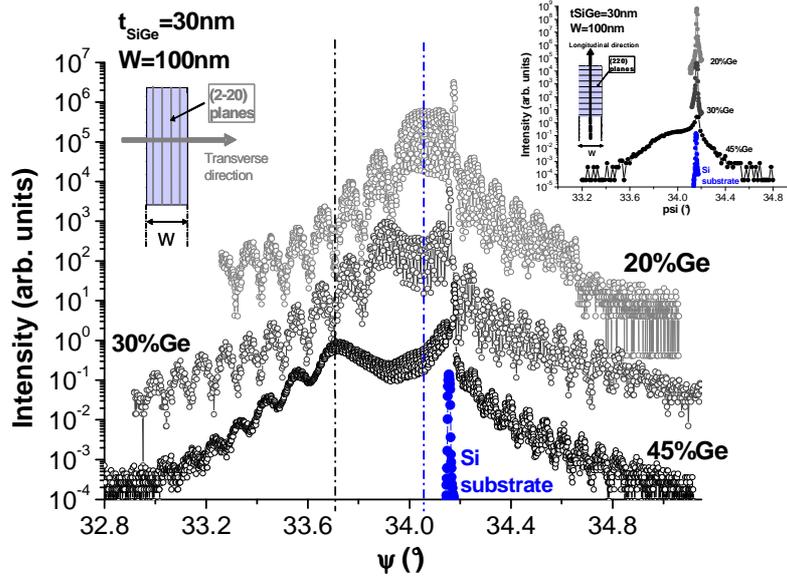


Fig. 4: (2-20) Bragg peaks of the Si/SiGe/Si stack ( $t_{\text{SiGe}}=30\text{nm}$ ,  $W_{\text{SiGe}}=100\text{nm}$ ,  $\% \text{Ge}=20,30,45\%$ ) and unstrained Si substrate. Inset: (220) Bragg peaks.

Finally, we have studied the influence of SiGe width for a fixed Ge fraction (20%) and a fixed SiGe layer thickness ( $t_{\text{SiGe}}=30\text{nm}$ ). We have plotted in Fig. 5 the radial scans for two different SiGe area width ( $W_{\text{SiGe}}=200, 100\text{nm}$ ). The Si substrate reference and the Bragg peak of unpatterned sample have also been plotted for comparison. The Bragg peaks of the unpatterned reference don't change in position for the two perpendicular directions, they are very close to the Si substrate reference. For non-etched SiGe/Si bilayer, the compressive SiGe layer and the upper Si layer conserves the same lattice parameter as the silicon on which the SiGe/Si bilayer has been epitaxially grown.

For the two patterned samples, there is no shift in the long line direction from the Si substrate. The shift in the transverse direction is greater for the 100nm width lines. The stress transfer mechanism is probably less efficient for a wider SiGe area. But we should also notice that the peak maximum is broader for the 100nm width line: on the one hand, the stress transfer is more efficient with a smaller SiGe area (the global strain value is larger), the other hand the Si tensile layer tends to relax more easily. For the 200nm width lines, the global strain value of the Si/SiGe stack is smaller, but there is probably less strain relaxation in the Si layer. *Taking into account the two mechanisms of stress transfer and stress relaxation, there should be an optimum value of the SiGe area width.* A planned sample with a 50 nm SiGe area width was not measurable due to process problems during etching. Mechanical and diffraction simulations will be performed to confirm the interpretations given in this report. The present measurements will give very nice calibration points to understand the relaxation in this complex structure.

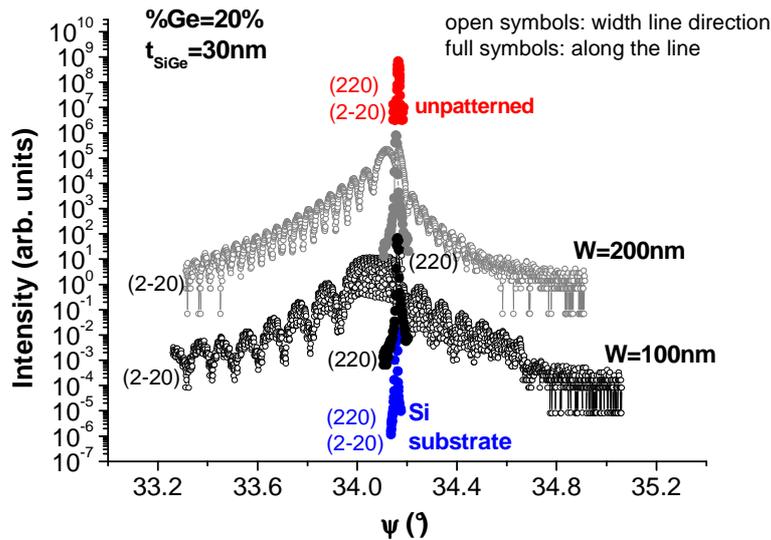


Fig. 5: (2-20) and (220) Bragg peaks of the Si/SiGe/Si stack ( $t_{\text{SiGe}}=30\text{nm}$ ,  $\%Ge=20\%$ ,  $W_{\text{SiGe}}=200, 100\text{nm}$ ), unpatterned Si/SiGe/Si stack ( $t_{\text{SiGe}}=30\text{nm}$ ,  $\%Ge=20\%$ ) and unstrained Si substrate.

To summarize the conclusions of this work:

- Grazing Incidence X-ray Diffraction (GIXRD) is a very powerful technique to measure the strain in reverse embedded SiGe structures.
- The tensile strain in the Si channel has been proved.
- Future work will be focused on the separation of the signals from the different layers in the Si/SiGe/Si stacking. The comparison of the measured strain with mechanical simulations is presently under way. The objective will be to obtain the strain profile in the Si top layer where electron transport will take place.
- These experiments gave very important information to find the best structural parameters that will optimize the stress transfer (the SiGe layer thickness  $t_{\text{SiGe}}$ , the width  $W_{\text{SiGe}}$  of the lines, the SiGe concentration). The influence of the strain on transport properties for this model transistor structures is also studied in parallel in the PhD of S. Baudot.

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