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Contrainte compressive dans les canaux de transistor
(Compressive stress in transistor channels)

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This experiment has been mainly focussed on an original technique to induce a compressive strain in the channel of Fully Depleted (FD)SOI MOSFETs thanks to an embedded buried nitride stressor. Strain measurements are performed by Grazing Incidence X-ray Diffraction (GIXRD) and compared to mechanical simulations. Both results are in agreement and prove that the strain level can achieve -0.6 % (-780 MPa) in the channel of a transistor, depending on the active region geometry and the nitride properties (intrinsic strain and thickness). This technique is thus very promising in order to boost pMOSFETs on thin films.
Most of the results have been presented in conference (0), full data analysis are still in progress.

Introduction

Fully Depleted (FD)SOI is a promising device architecture for Low Power 22 nm MOSFETs technologies, mainly because of the low leakage current and the record matching performance already demonstrated (1,2). Some effective techniques were already experienced to boost the ON current through the strain in FDSOI, especially for nMOS (Contact Etch Stop Layer, sSOI substrates…) (3). However, for pMOS, the widely used embedded SiGe source/drain process is very challenging to integrate on FDSOI because of the small active body thickness. There is thus a huge interest for new process techniques to induce a compressive strain in the channel of the device.

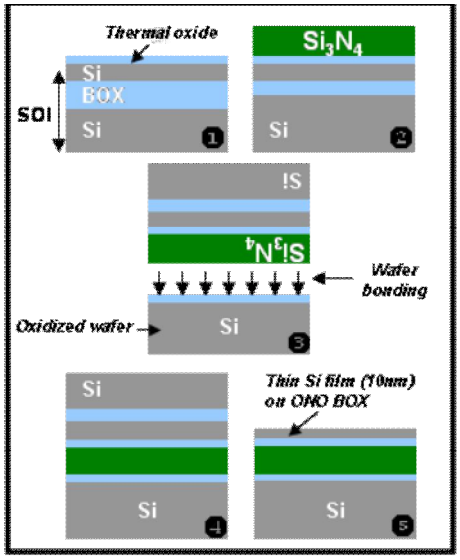
In this study, an original embedded buried nitride stressor structure is proposed and characterized from the structural point of view. It is based on a stress transfer from a buried nitride stressor (embedded in the Buried Oxide (BOX) of the substrate) to the transistor channel. The great interest of such stress transfer techniques is that the strain could be significant even for small channel dimensions, i.e. for nominal devices.

In order to check that this method can be applied to small dimensions, we measured accurately the strain in sub-100 nm tests structures by Grazing Incidence X-Ray Diffraction. The strains in nano-structured and thin films are generally obtained with several direct characterization techniques: Raman spectroscopy (4,5), High Resolution X-ray Diffraction (6,7), Grazing Incidence X-Ray Diffraction (GIXRD) (8), or Transmission Electron Microscopy (TEM) based methods such as Convergent Beam Electron Diffraction or High Resolution (9). However, for this last technique, the lamella preparation induces a strain relaxation and fine mechanical simulations must be performed in order to interpret the data (10). For Raman spectroscopy, the complete lattice strain tensor is very difficult to obtain without any assumption (4). Among the different aforementioned techniques, GIXRD allows characterizing the complete lattice strain tensor with a high accuracy, without any assumption or special sample preparation.

In this study, we use GIXRD to check quantitatively the efficiency of the stress transfer from the nitride layer. We will present the sample fabrication process in part I and II, then the GIXRD strain measurements obtained for patterned samples will be given in part III. Finally,

the comparison between the GIXRD experimental results and finite element mechanical simulations will be given in part IV.

Wafer fabrication



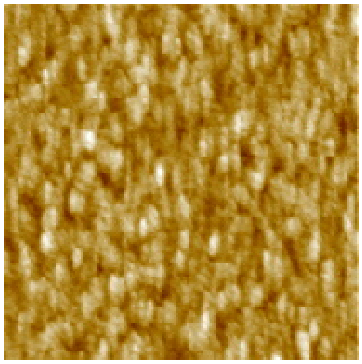


Figure 1a. (left) Schematic view of the SOI substrate made with an ONO buried stack.
Figure 1b. (top) AFM scans (1x1µm², Z_{max}=5 nm) on the Si_3N_4 surface for the as-deposited layer (RMS = 0.24 nm, PV = 1.96 nm).

We fabricated SOI wafers with an Oxide/Nitride/Oxide (ONO) buried stack instead of the classical SiO_2 BOX. These specific substrates were made using the Bonded and Etched-back SOI (BESOI) technology (Figure 1a). The silicon nitride layers were obtained by Low Pressure Chemical Vapour Deposition (LPCVD) on 200 mm SOI donor wafers which were previously oxidized (3 nm SiO_2 layer). Two Si_3N_4 thicknesses were processed: 30 nm (deposited at 750 °C) and 140 nm (deposited at 780 °C). Atomic Force Microscopy (AFM) was used to characterize the Si_3N_4 surface roughness (1x1 µm² scans): RMS values below 0.3 nm were measured on the as-deposited layers (Figure 1b). This very flat surface allows a direct chemical bonding without polishing process. The base wafers were prepared by thermal growth of 5 nm thick silicon dioxide layers. We found that a standard RCA cleaning protocol on both donor and base wafers is sufficient for hydrophilic nitride bonding (11). A spontaneous bonding between thermal oxide and silicon nitride layers occurs at room temperature. The bonded pair was then annealed at high temperature (950 °C) in order to reinforce the bonding interface. To finish the process, the Si substrate and the SiO_2 BOX of the SOI donor wafer are removed by grinding and chemical etching. The final structure consists in a thin Si film (6 nm after thinning steps) on an ONO buried stack with 4/26/6 nm and 4/140/6 nm thicknesses, measured by ellipsometry and confirmed by TEM (Figure 2).

Test structure patterning

The 6 nm thick top Si layer and the ONO stack were etched by RIE to form a grid of 4 mm long and W=50,100,200 nm wide lines (see Figure 2). The objective of the etching is to relax the intrinsic tensile strain of the nitride layer and to transfer a compressive strain into the top Si layer (12). This concept is similar to the “Reverse Embedded SiGe” method (13,14). However, it is more compatible with thin film technologies because the stressor is directly integrated inside the BOX.

The efficiency of the stress transfer depends on the one hand on geometrical dimensions and on the other hand on the initial intrinsic tensile strain of the nitride layer before etching. The intrinsic tensile strain of the nitride layer is very dependent on the deposition process. The value of this intrinsic strain determines the maximum strain that could be transferred to the SOI layer for the optimised geometrical dimensions. In this work, we have mainly

investigated the influence of two geometrical dimensions: the nitride layer thickness and the active area width.

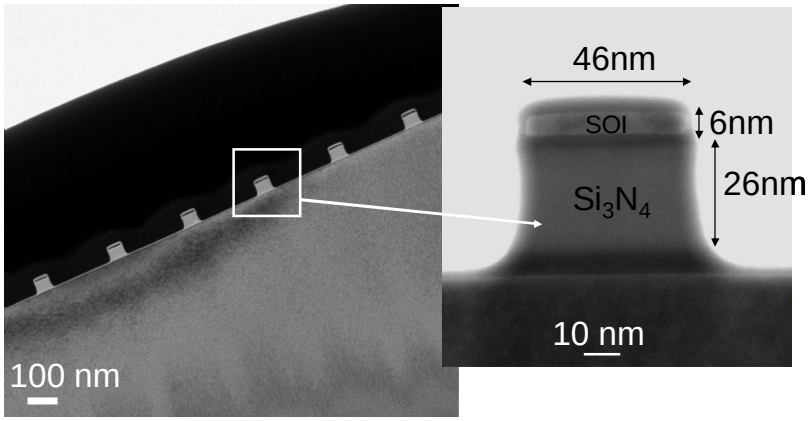


Figure 2. TEM cross-section of a sample with W=46 nm narrow lines and 6/4/26/6 nm Si/oxide/nitride/oxide thicknesses. The right figure is obtained in a Scanning TEM mode.

GIXRD Characterization

The X-ray energy is 11 keV. Grazing incidence (α_i=0.12°) and emergence angles (α_f=0.24°) close to the critical angles of total reflection allow measuring the diffraction of the (220) and (2-20) planes perpendicular to the surface of the top SOI layer (see inset of Figure 4a). Larger grazing angles (α_i=0.3°, α_f=0.6°) are used to go through the amorphous nitride layer, in the substrate. The Si substrate gives an internal stress-free reference in the samples both in position and width allowing to check the setup alignment and the resolution function, and to decrease the error bar of the strain measurement. The ψ_{SOI} (ψ_{Sub}, respectively) Bragg peak angles of the SOI layer and substrate respectively are obtained by the optimization of intensity with radial and transverse scans at given grazing angles. Applying the Bragg law to the SOI layer and Si substrate, we get for the in-plane strain in the SOI layer:

$$\varepsilon = \sin(\psi_{Sub}/2)/\sin(\psi_{SOI}/2) - 1 \qquad [1]$$

This equation shows that the strain can be directly deduced from the detector angular position. The measurement of the (220) planes allow getting the strain in the so-called "longitudinal" direction; whereas the (2-20) planes give the strain in the "transverse" direction (see inset of Figure 4a).

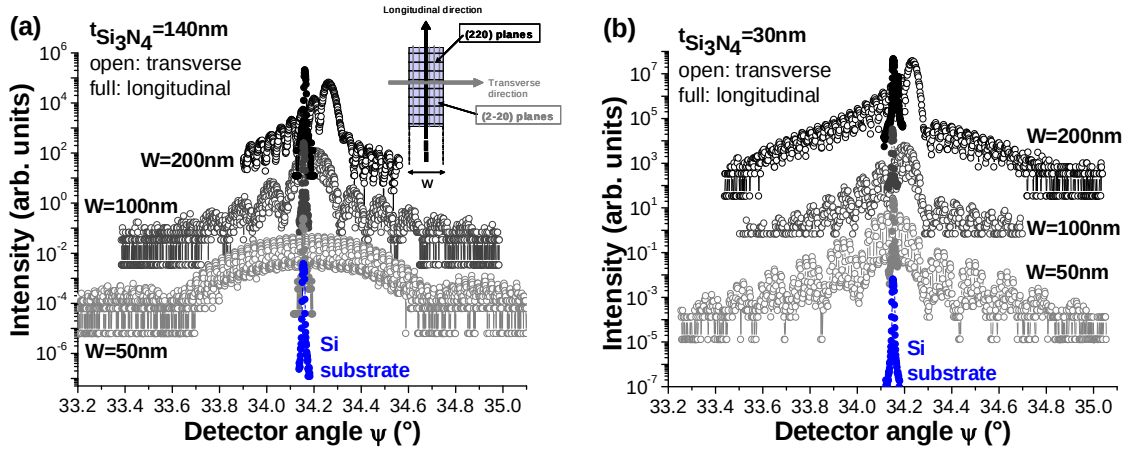


Figure 4. Measurements of (220) and (2-20) Bragg peaks of W=50,100,200 nm SOI lines and Si substrate with a) 140 nm (left figure) and b) 30 nm (right figure) thick nitride layers. Only one peak corresponding to the Si substrate response is plotted at the bottom of each figure (always measured at the same position for each W). Inset: Strain measurement directions and top view of the corresponding crystallographic planes.

The diffracted intensities corresponding to the planes along and perpendicular to the lines are shown in Figures 4a and 4b for 140 nm and 30 nm nitride thicknesses respectively and for different line widths. The Bragg peak relative to the Si substrate is also plotted as reference (the lower sharp peaks). Along the lines, all the Bragg peaks of the top Si are at the same detector angular position ψ as the Si substrate. There is thus no significant strain in this direction whatever the line width and the nitride thickness. In the other direction, the Bragg peaks of the Si on ONO are shifted from the Si substrate position toward larger ψ angles. This demonstrates that the Embedded Buried Nitride technique is effective to induce a compressive strain in the narrowest direction. We extracted the average of the strain in the Si layer using [1] for each line width and nitride thickness. The experimental results have been plotted in Figure 6 (symbols). This figure shows a slightly higher compressive strain in the Si channel with 140 nm than with 30 nm thick nitride. Moreover, this strain surprisingly increases when the active region increases, at least until W=200 nm. To confirm these measurements and to predict the behavior above W=200 nm, we used finite element mechanical simulations.

Mechanical Simulation

Finite element simulations have been performed with the ANSYS tool. The simulated structure was shown in Figure 2 and the mechanical inputs were the intrinsic strain of the nitride layer (s=1100 MPa) and the elastic coefficients of the nitride (Young modulus E=160 MPa and Poisson ratio ν= 0.24). The simulations were done for devices with 30 nm or 140 nm thick nitride and different line width W (see Figure 6). Only the right half of the device was simulated because of the structure symmetry. There is a high uncertainty in the published values of the elastic coefficients and intrinsic strain of the nitride layers depending a lot on the deposition process. The influence of these uncertainties on the strain is illustrated in Figure 6a considering independent variations of the nitride parameters given previously. As shown in Figure 6b, GIXRD measurements and several finite element calculations with realistic values for input parameters are in very good overall agreement for small W.

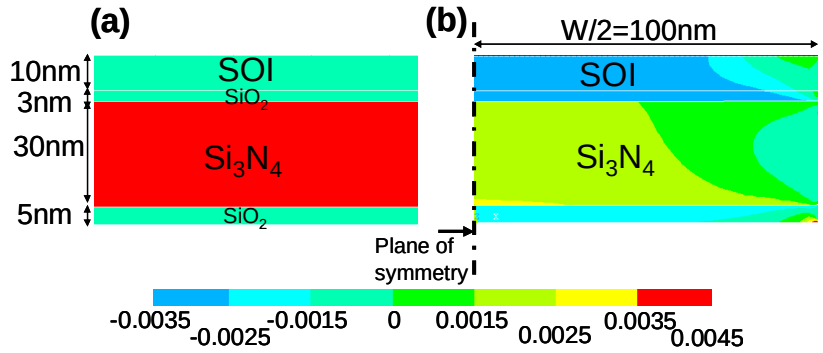


Figure 5. Simulation of the lateral strain in the Embedded Buried Nitride structure (a) before and (b) after the W=200 nm large active area patterning. Before the etching, the strain in the nitride is uniform and tensile, and there is no strain in the SOI layer. After etching, the tensile strain of the nitride is reduced, and compressive strain is induced in the SOI layer.

The simulation results confirm the aforementioned mechanism of the strain transfer. Indeed, the etching of the SOI/$Si0_2$/Si_3N_4/$Si0_2$ stack relaxes the strain of the Si_3N_4 layer from the edges (compare the red color before the etching in Figure 5a and the green/blue color after the etching in Figure 5b) transferring a compressive strain in the SOI layer (see the central blue region in Si in Figure 5b).

The simulations highlight a non monotonous behaviour of the strain vs. the active area width (W), with a strain optimum in the region 150 nm<W<800 nm, depending on the nitride thickness. This optimum is due to the balance between the aforementioned Si compression caused by the nitride relaxation (responsible for the growing part of the curve for large areas) and the Si relaxation itself (responsible for the drop of the curve for narrow patterns). This Si relaxation is also due to the etching and evidenced in Figure 5b, where we can see border effects in the SOI layer (green region). That is why, for sub-100 nm patterns, this border effect leads to a limited final transferred strain in the SOI layer (see Figure 6b).

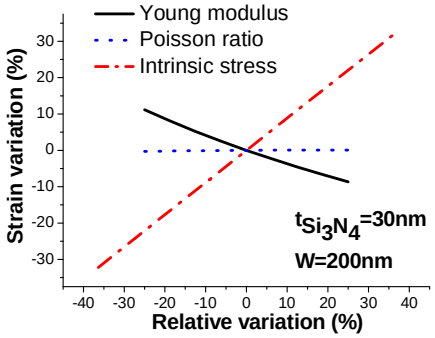


Figure 6a. Variation of the average strain in the SOI layer induced by variation of the inputs of the mechanical simulations.

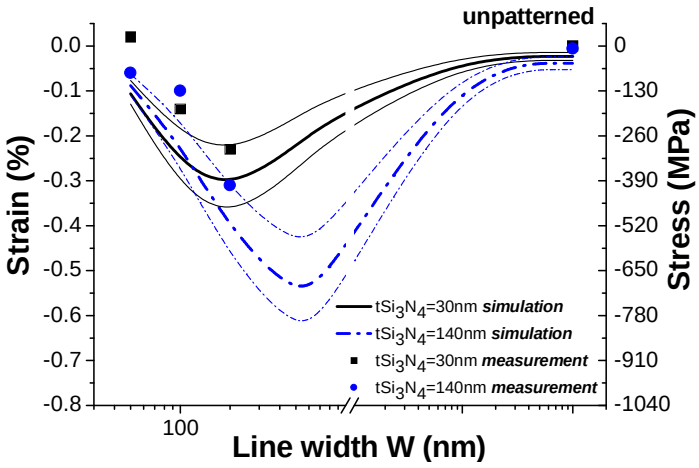


Figure 6b. Average strain in the SOI layer in the line vs. the line width for 30 nm and 140 nm nitride thicknesses: comparison between GIXRD measurements and finite element simulations. Three set of elastic coefficients values have been taken into account for the simulations (s=1100 MPa, E=160MPa, v=0.24), (s=700 MPa, E=120MPa, v=0.24) and (s=1500 MPa, E=200MPa, v=0.24).

Conclusion

We propose an original technique to induce a compressive strain in the channel of FDSOI MOSFETs thanks to an Embedded Buried Nitride stressor. The interest of this method is evidenced by the fabrication and strain measurement of a patterned substrate having a buried nitride layer. The in-plane deformations measured by GIXRD are in quantitative agreement with finite element mechanical simulations which show that the channel strain can reach -0.6 % (-780 MPa) with optimized geometrical features i.e. the nitride and top Si thicknesses, and the active area dimensions. A proper design adjustment must thus allow tuning the 2D strain in the channel of FDSOI MOSFETs in order to, in turn, boost CMOS performance.

References

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