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Amorphous ternary rare-earth gate oxides for future integration in MOSFETS.

The introduction of hafnium-based gate oxides in nanoscaled MOSFETs has been realized for the 45 nm technological node by the leading chip manufacturers, and recently announced for the 32 nm generation. However, further device scaling, for which an equivalent oxide thickness (EOT) equal to or below 0.9 nm will be required, may be unfeasible with these materials due to their relatively low dielectric constants *k* below 20. Therefore, investigation of so-called higher-*k* dielectrics with *k* values higher than 20 is needed. Rare-earth ternary oxides are among the promising candidates for higher-*k* applications. Amorphous thin films of rare earth scandates ($RE\mathrm{ScO}_3$ *RE*=La, Gd, Sm, Dy) offer *k* values ranging from 20 to 32 [e.g. 1,2], large optical band gaps (>5 eV), and band offsets to silicon (2–2.5 eV) [3]. Additionally, they distinguish themselves by their high thermal stability of the amorphous phase ranging from 800 °C to 1000 °C [e.g. 1, 2]. During the growth of $LaScO_3$ gate stacks on silicon it was shown, that a silicate formation takes place at the interface substrate-oxide film [4]. In fact, XPS analyses reveal the existence of silicate near the interface, even for films deposited at temperatures as low as 200 °C. XPS using AlKα source cannot provide a suitable depth resolution to distinguish between surfacial or interfacial silicate. In addition normal XPS information depth is limited to 5 nm and therefore cannot analyze buried interfaces in the range of 3-6 nm depth or even deeper.

The powerful technique HAXPES (hard X-ray photoelectron spectroscopy) allows determining the composition and thickness on the nanoscale of gate stacks of higher-*k* materials (e.g. $LaLuO_3$) on Silicon or Germanium. This investigation should give an inside into the formation of the interfacial layer between the substrate and the oxide film which influences the properties of these gate stacks in devices. The interfacial layer properties vary with the growth conditions (e.g. substrate temperature) of the oxide thin films, which is already known and shown in previous studies [4]. Here we want to analyse samples, which were thermally treated under different temperatures after deposition. This treatment is necessary to optimize the electronic properties of the device, but it is not clear right now what happens to the interface during annealing. Temperature induced formation of silicates at the interface occurs during deposition under different temperature conditions, therefore we expected to find similar results on the annealed samples.

The samples were prepared in Juelich with molecular beam deposition under the same conditions. They consist of $LaLaO_3$ (LLO) as high-k material (10nm thick) on Silicon with 15nm TiN capping layer. After MBD deposition samples were annealed with different temperatures. During our beamtime we investigated the sample as deposited and 4 samples with additional thermal treatment (400°C, 600°C, 800°C, and 1000°C). Core levels of Si, La, Lu, Ti, N and O were measured with 10keV, 12keV, and 14keV, respectively.

Figure 1 shows the Si1s core-level for the sample as deposited and 1000°C for the photon energies 10keV, 12keV, and 14keV. Both samples were deposited in the same way and had the same layered structure before one of them was annealed. If the overall thickness of the stack (TiN and LLO) stays the same during the temperature step the information depth should be the same for both samples at the same distinct photon energy. Both samples show the Si±0 of the Si substrate at all energies. Therefore the information depth is larger than 25nm. The sample additionally annealed at 1000°C has a second peak at a higher binding energy which

corresponds to either SiO_2 or a silicate. Higher photon energy and therefore larger information depth changes the ratio of these two Si peaks as expected. The substrate peak becomes higher with higher photon energy.

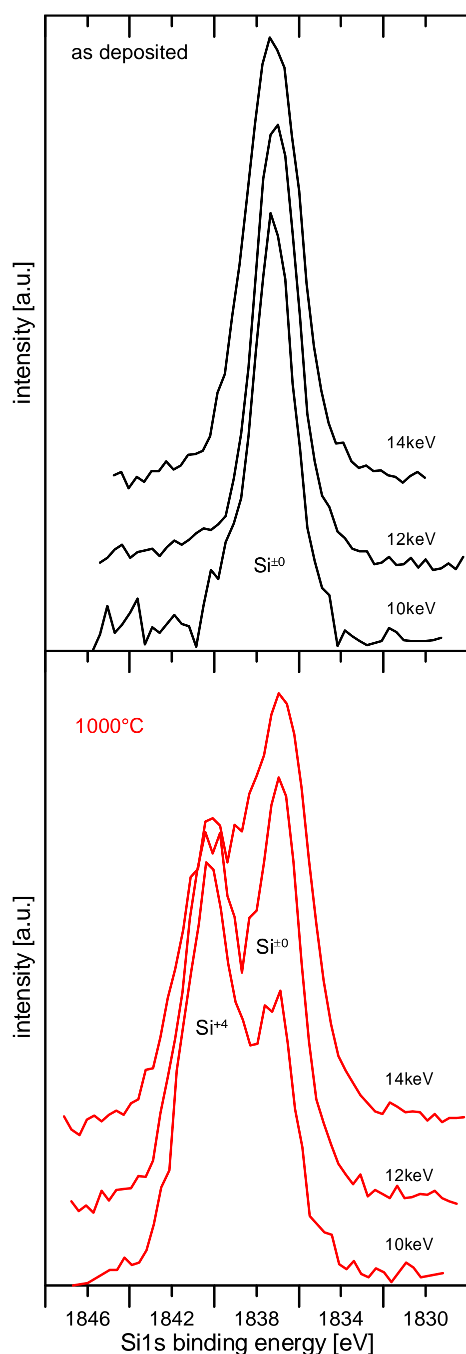

Figure 1:
Si 1s core levels for sample as deposited (top) and 1000°C (bottom) for three different photon energies.

The formation of a second Si compound during annealing is in agreement with the observed formation of such a compound during different temperature dependent growth conditions. Higher temperatures favours the mobility of Si and/or O and leads to a formation of a Si containing compound at the substrate/oxide interface.

Mixing of the deposited materials during annealing could result in e.g. La-Lu silicate formation, which should be visible in different La and/or Lu core level compounds.
The measurement statistics of La and Lu core levels were not good enough to gain suitable results for both elements. The cross section of La and Lu is comparable with that of Si. We wonder about the relatively high Si countrate with respect to La and Lu, because Si should be in greater depth than La and Lu. It is possible that Si is also apparent at the LLO/TiN interface due to high Si mobility within oxides. Therefore we need higher depth resolution in order to find out, where the Si is located. This could be achieved by measuring more than one core level per element per photon energy.

Overall conclusion of our beamtime is that we have very successful experiments with HAXPES, but we need to optimize the measurement procedure to get the maximum information. We would like to thank Juan and German for their great help and useful discussions.

References

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