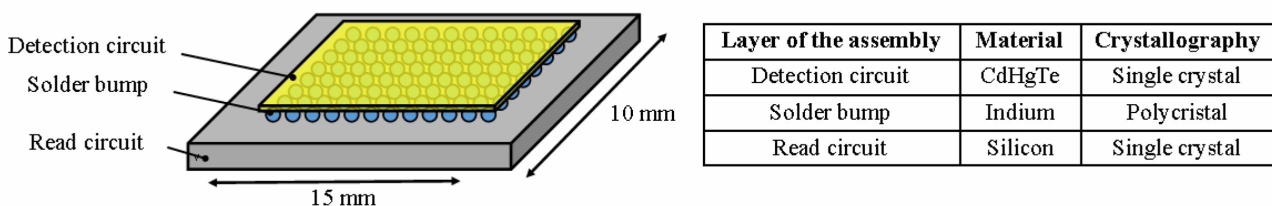
<table>
<tr><td> </td><td>Experiment title: Stress analysis on multi-layers electronic assemblies to improve reliability, save ressources and minimise recycling and pollution</td><td>Experiment number:
32-02 802</td></tr>
<tr><td>Beamline:
BM32</td><td>Date of experiment:
from: 27-04-2017 to: 02-05-2017</td><td rowspan="2">Date of report:
19-10-2017
Received at ESRF:</td></tr>
<tr><td>Shifts:
15</td><td>Local contact(s):
Jean-Sébastien Micha</td></tr>
<tr><td colspan="3">Names and affiliations of applicants (* indicates experimentalists):
Raphaël Pesci, Anne-Laure Lebaudy
ENSAM-Arts et Métiers ParisTech, Laboratoire LEM3 UMR CNRS 7239, 4 rue Augustin Fresnel, 57078 Metz cedex 3.
Email: raphael.pesci@ensam.eu</td></tr>
</table>

Report

Aims of the experiment and scientific background

3D integration is a promising solution to the electronic circuits miniaturization. The interconnections occur in 3 dimensions by using the faces of the chip stack to make the connections between the slices. This technology allows to increase the performance of circuits without going through the miniaturization of components and the features diversification using heterogeneous integration. A major benefit is the significant cut in the energy consumption through the replacement of long horizontal connections by shorter vertical connections. Nevertheless, this architecture induces extreme thermomechanical stresses during the manufacturing process which can generate damages in several layers of the assembly. Recycling defective CdHgTe based infrared detectors containing heavy metals such as mercury and cadmium is complex and detrimental to the environment. A particularity of these components is the working temperature of 77K which is critical for the reliability of the electronic assembly and amplifies several failure modes as the detection circuit warpage or solder bump crack. In order to understand these defects, several strain/stress analyses have been carried out at room temperature (293K) and cryogenic temperature (77K) using laboratory X-ray diffraction. This assembly consists of three layers presented Figure 1: a single crystal of CdHgTe composed of a 30µm width pixel matrix, a polycrystalline interconnexion layer constituted of an indium solder field underfilled with amorphous epoxy and a single crystal silicon substrate.



Layer of the assembly	Material	Crystallography
Detection circuit	CdHgTe	Single crystal
Solder bump	Indium	Polycristal
Read circuit	Silicon	Single crystal

Figure 1 CdHgTe based IR detector structure

A specific method available for single crystal analysis has been optimised for such multilayers architecture using a laboratory four circle diffractometer to obtain the stress values in the CdHgTe layer and in the below silicon substrate. Nevertheless, the available energy in laboratory don't allow the simultaneously analysis of the CdHgTe detection circuit and the silicon substrate. And then, this technic allows a millimetric resolution which don't allow the pixel to pixel study of the CdHgTe detection circuit at a micrometric scale. So the aim of the experimental campaign on BM32 was to map some pixel of the CdHgTe circuit with a high energy microbeam in order to get for each point simultaneously a Laue pattern of CdHgTe, and Si to obtain strain value the both layers at room temperature and close to -196°C (running temperature of the detector) at a micrometric scale. Indeed, we expected that the strains/stresses were increased at low temperature due to heterogeneous thermal expansion and dilatation of the different materials. We proposed to realise Laue microdiffraction at several location of the assembly (centre and corner of the CdHgTe detection circuit) coupled with XRF technique to localise solders on the assembly in order to link stress mapping with the geometry below the CdHgTe detection circuit.

Experimental method

A specific cooler has been designed and adapted on BM32 device. The cryostat is placed on a table allowing x, y and z motion (Figure 2).

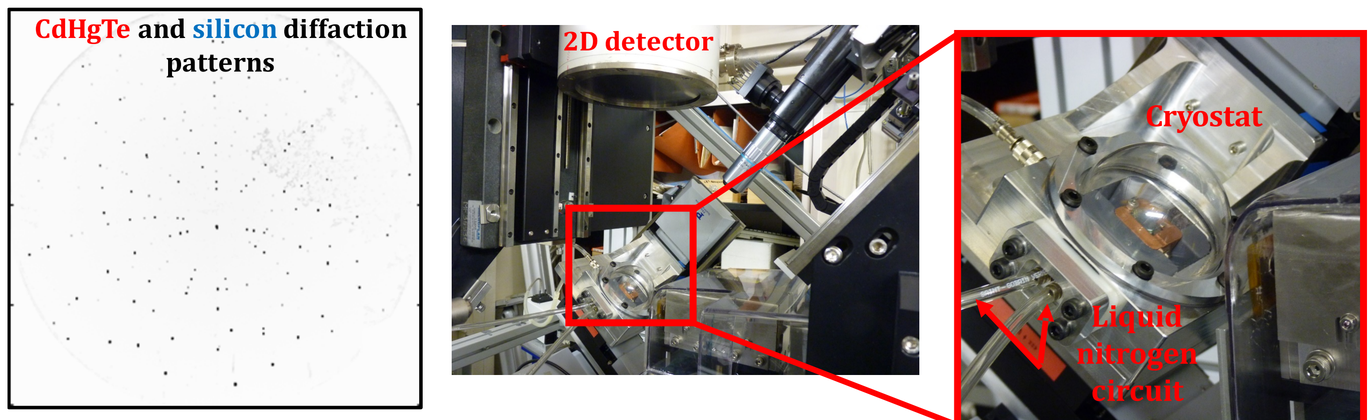


Figure 2 Diffraction patterns of the structure and experimental set up on the BM32 beamline

The sample is fixed on a copper part cooled with an internal constant liquid nitrogen flow. A half-sphere partially transparent to X-rays above the sample and a vacuum circuit protects the system against ice forming. This geometry allowed an optimal accessibility of the incident/diffracted beam. So ambient and cryogenic microLaue mappings have been conducted in both CdHgTe and silicon in different zones in order to observe the thermal strain gradient, calculate the strain/stress and compared to the FEM model previously developed. X-ray fluorescence of the sample is also analysed with a specific detector available on the beamline. A focused white beam, 5 to 19keV and 0,7µm x 0,7µm, was used.

Results

An example of the spot displacement observed for CdHgTe is given in Figure 3 at room temperature and 77K considering the same location in the CdHgTe circuit. The amplification of the spot displacements at very low temperature is due to higher strain induced in the CdHgTe and valid the FEM model prediction. With X-ray fluorescence, it is possible associate each value to one position in each pixel of the CdHgTe circuit (above the indium bumps or around).

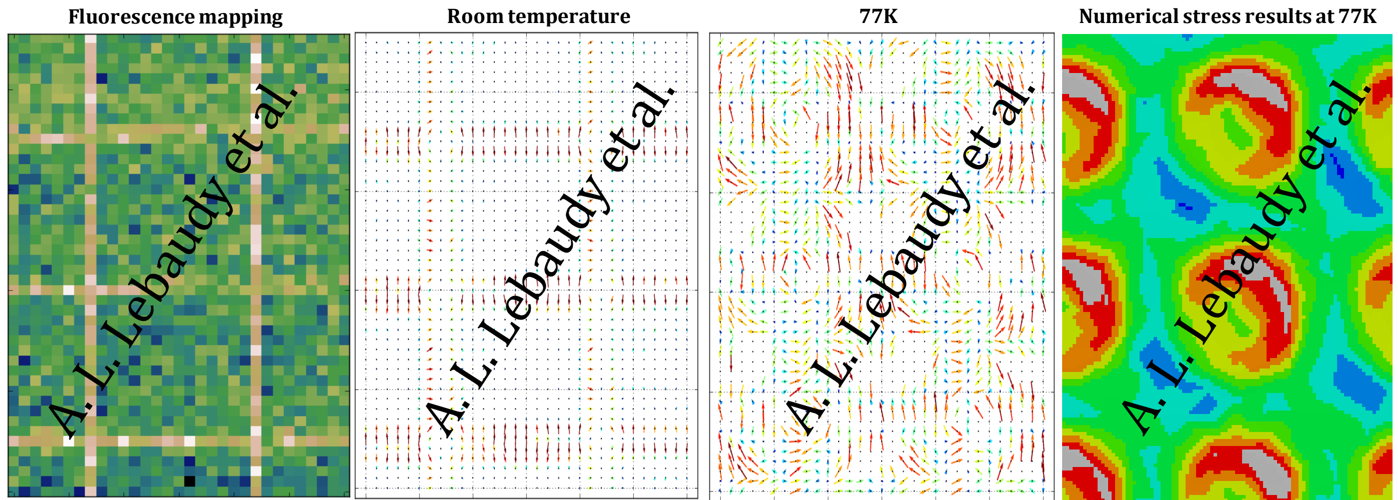


Figure 3 Mapping of the diffraction CdHgTe spot displacements linked to the geometry of the detection circuit

With the hypothesis $\sigma_{zz}=0$, stress values can be computed for each point of the mapping. The values are between -23MPa and 30MPa at 77K and in accordance with numerical results.

All this work will be presented during international conferences and published in international scientific journal (Acta Materialia).